WHAT IS CLAIMED IS:

1. A MOS transistor formed on a semiconductor material of a first conductivity type, the transistor comprising:

a layer of material of the first conductivity type formed on the semiconductor material, the layer of material including silicon, germanium, and carbon;

spaced apart source and drain regions of a second conductivity type formed in the layer of material;

a channel region located between the source and drain regions;

an insulation layer formed over the layer of material; and

a gate formed on the insulation layer over the channel region.

2. The MOS transistor of claim 1 wherein the layer of material has a substantially uniform concentration of carbon atoms.

3. The MOS transistor of claim 1 wherein the layer of material has a non-uniform concentration of carbon atoms.

4. The MOS transistor of claim 3 wherein the layer of material further includes:

an upper region of carbon that has a first concentration of carbon atoms; and

a lower region of carbon that has a second concentration of carbon that is less than the first concentration, the lower region lying below and contacting the upper region.

5. The MOS transistor of claim 1 and further including a trench isolation region, the trench isolation region electrically isolating the semiconductor material from laterally adjacent areas.

6. The MOS transistor of claim 5 wherein the trench isolation region has a top surface, the layer of material has a bottom surface, and the top surface of the trench isolation region and the bottom surface of the layer of material are in substantially a same plane.

7. The MOS transistor of claim 4 wherein the trench isolation region has a top surface, the layer of material has a bottom surface, and the top surface of the trench isolation region and the bottom surface of the silicon germanium carbon layer are not in a same plane

8. The MOS transistor of claim 1 wherein the layer of material includes a layer of silicon substantially free of carbon and germanium, and an overlying layer of that includes silicon, germanium, and carbon.

9. The MOS transistor of claim 1 and further comprising a cap silicon layer formed on the layer of material, the insulation layer being formed on the cap silicon layer.

10. A method of forming a MOS transistor on a semiconductor material of a first conductivity type, the method comprising the steps of:

forming a layer of material of the first conductivity type on the semiconductor material, the layer of material having silicon, germanium, and carbon;

forming an insulation layer over the layer of material;

forming a layer of conductive material on the insulation layer;

etching the layer of conductive material to form a gate; and

forming spaced-apart source and drain regions of a second conductivity type in the layer of material on opposite sides of the gate.

11. The method of claim 10 wherein the forming a layer of material step includes the step of growing the layer of material on the semiconductor material.

12. The method of claim 10 wherein the forming a layer of material step includes blanket depositing a layer of silicon germanium carbon over the semiconductor material.

13. The method of claim 10 wherein

an isolation region adjoins the semiconductor material, the isolation region having a top surface; and

the forming a layer of material step includes the step of selectively epitaxially growing the layer of material on the semiconductor material, the layer of material having a top surface that lies below the top surface of the isolation region.

14. The method of claim 13 wherein the semiconductor material has a bottom surface that is substantially coplanar with the top surface of the isolation region.

15. The method of claim 10 wherein the forming a layer of material step includes the steps of:

removing a portion of the semiconductor material to expose an etched surface of the semiconductor material; and

growing the layer of material on the etched surface of the semiconductor material.

16. The method of claim 10 wherein the forming a layer of material step includes the steps of:

removing a portion of the semiconductor material to expose an etched surface of the semiconductor material; and

blanket depositing a layer of silicon germanium carbon over the etched surface of the semiconductor material.

17. The method of claim 12 wherein the forming a layer of material step includes the steps of:

removing a portion of the semiconductor material to expose an etched surface of the semiconductor material, the etched surface of the semiconductor material lying below the top surface of the isolation region; and

epitaxially growing the layer of material on the etched surface of the semiconductor material.

18. The method of claim 15 and further comprising the step of forming a layer of cap silicon on the layer of material prior to the formation of the insulation layer.

19. The method of claim 10 wherein the layer of material has a substantially uniform concentration of carbon atoms.

20. The method of claim 10 wherein the layer of material has a non-uniform concentration of carbon atoms, and includes a surface region of a heavy concentration of carbon.